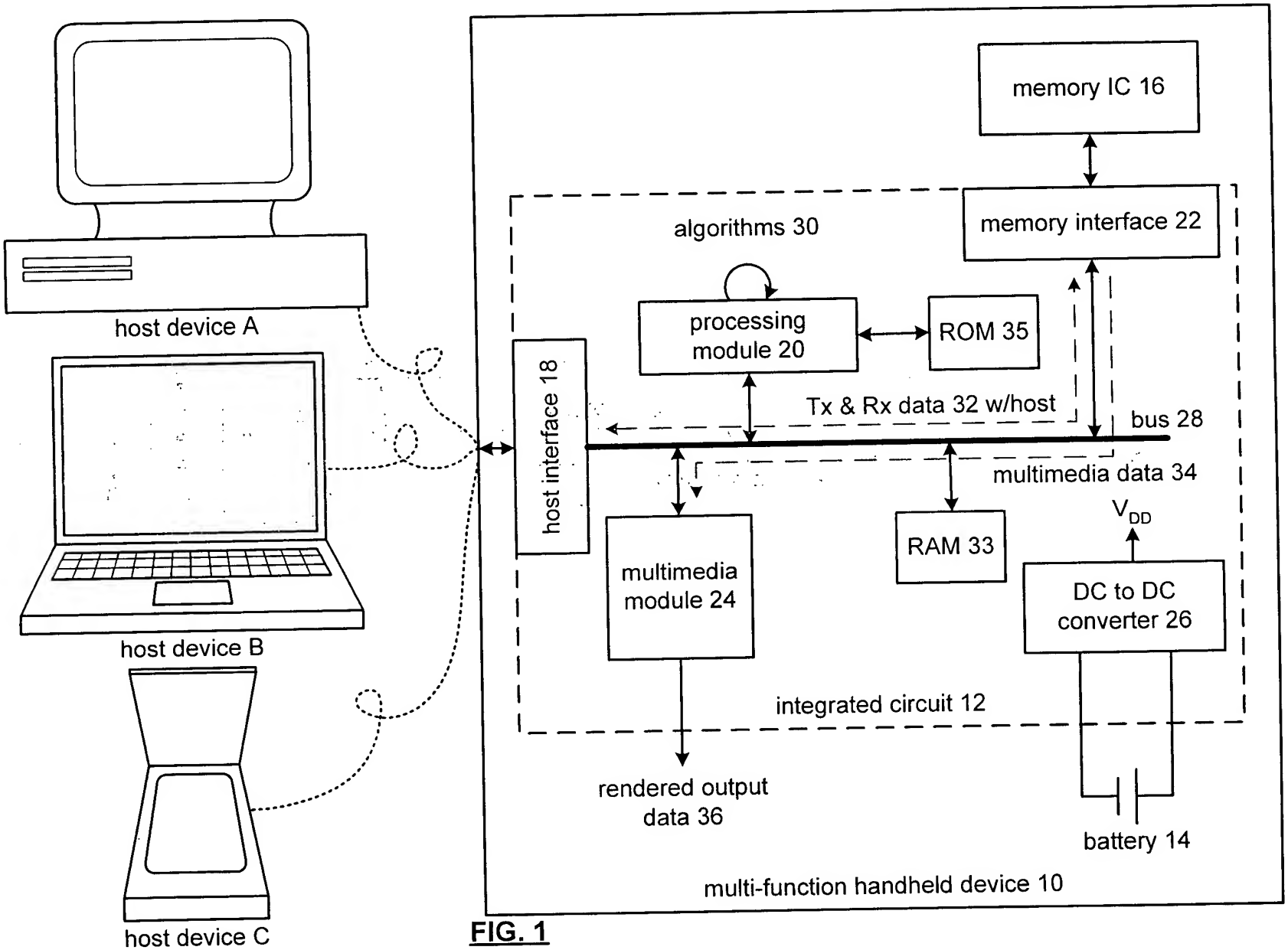
host device A
host device B
host device C
memory IC 16
memory interface 22
algorithms 30
processing module 20
ROM 35
host interface 18
Tx & Rx data 32 w/host
bus 28
multimedia data 34
$V_{DD}$
RAM 33
multimedia module 24
DC to DC converter 26
integrated circuit 12
rendered output data 36
battery 14
multi-function handheld device 10

FIG. 1

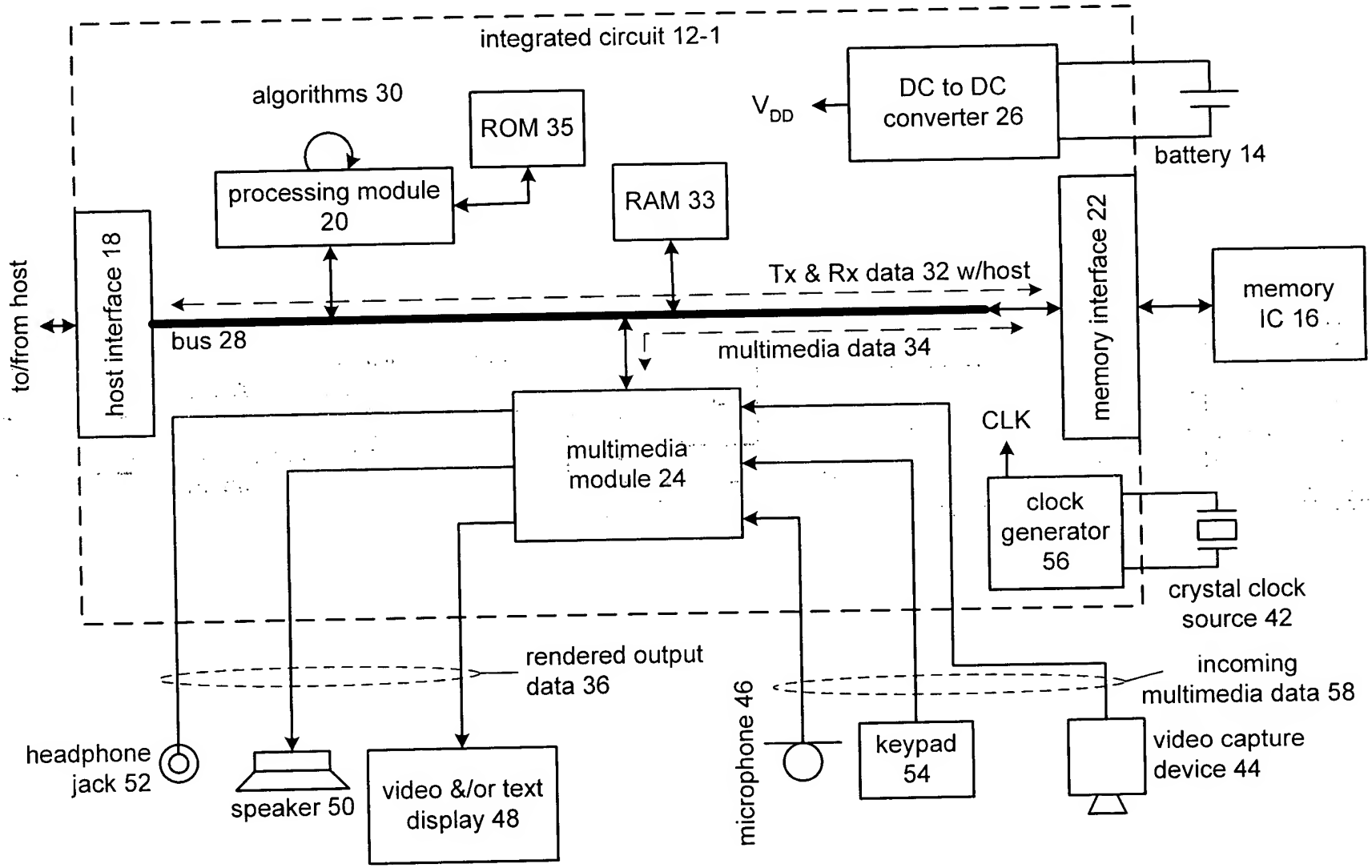


**FIG. 2**

**multi-function handheld device 40**

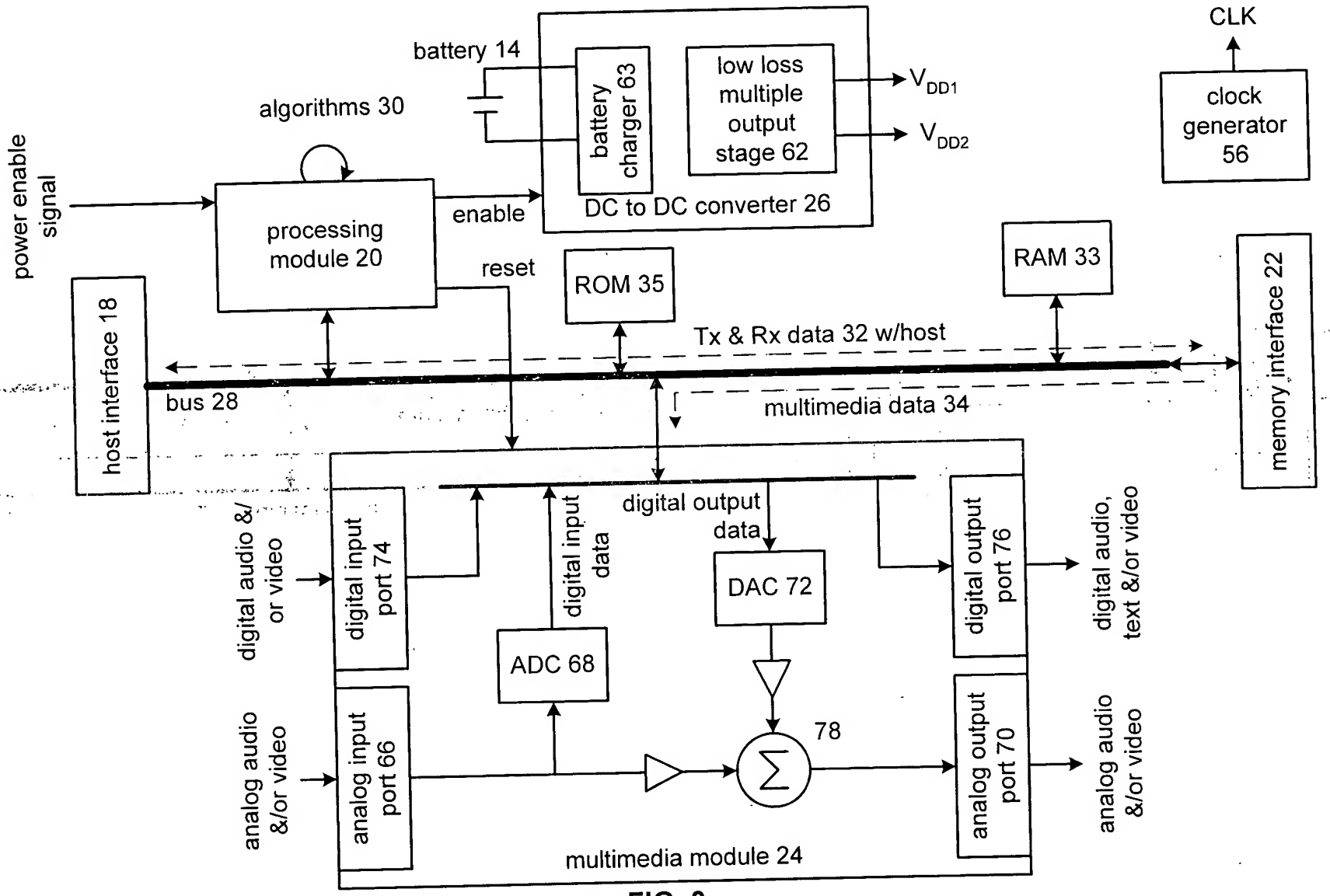


**FIG. 3**

**integrated circuit 12-2**

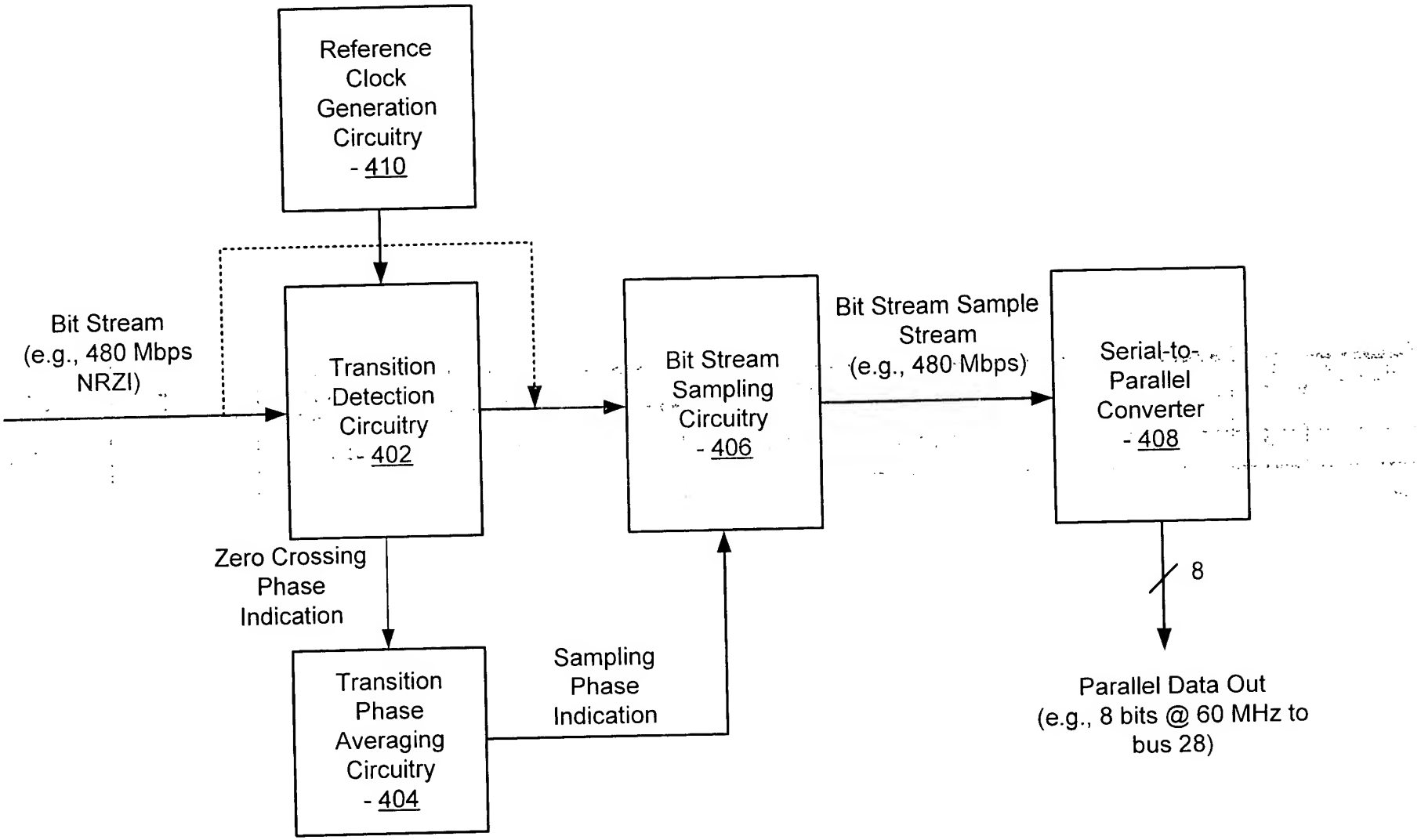


**FIG. 4**
**Host Interface - 18**

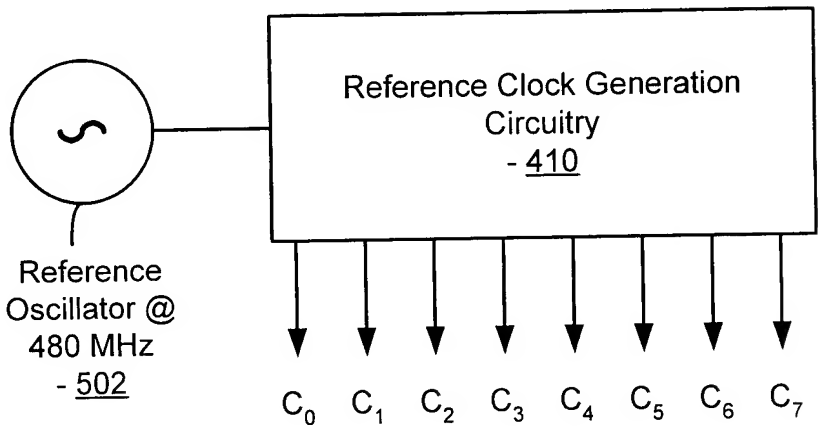


FIG. 5A

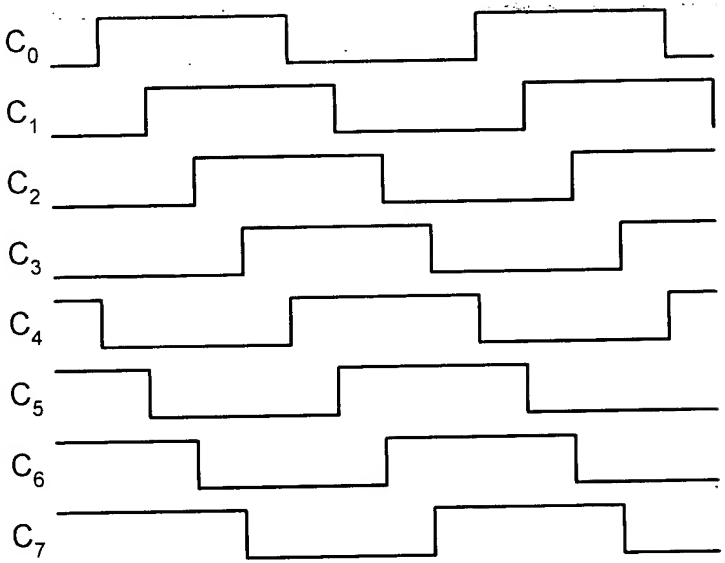


FIG. 5B

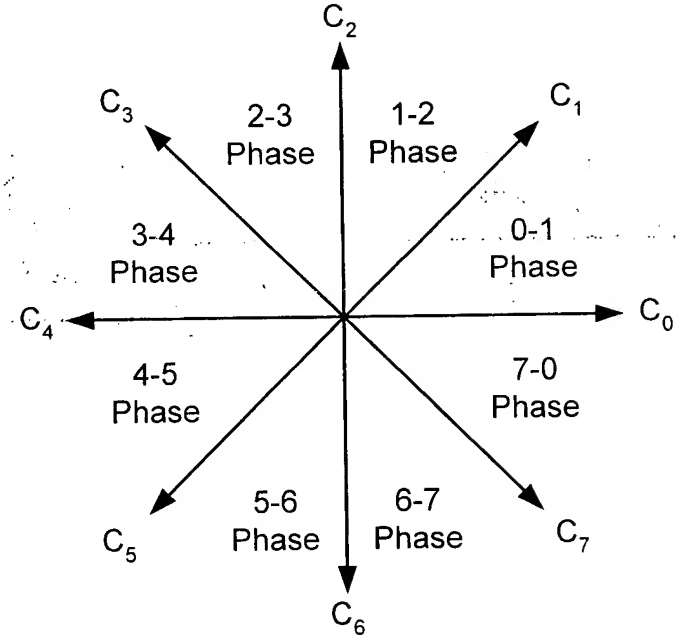


FIG. 5C

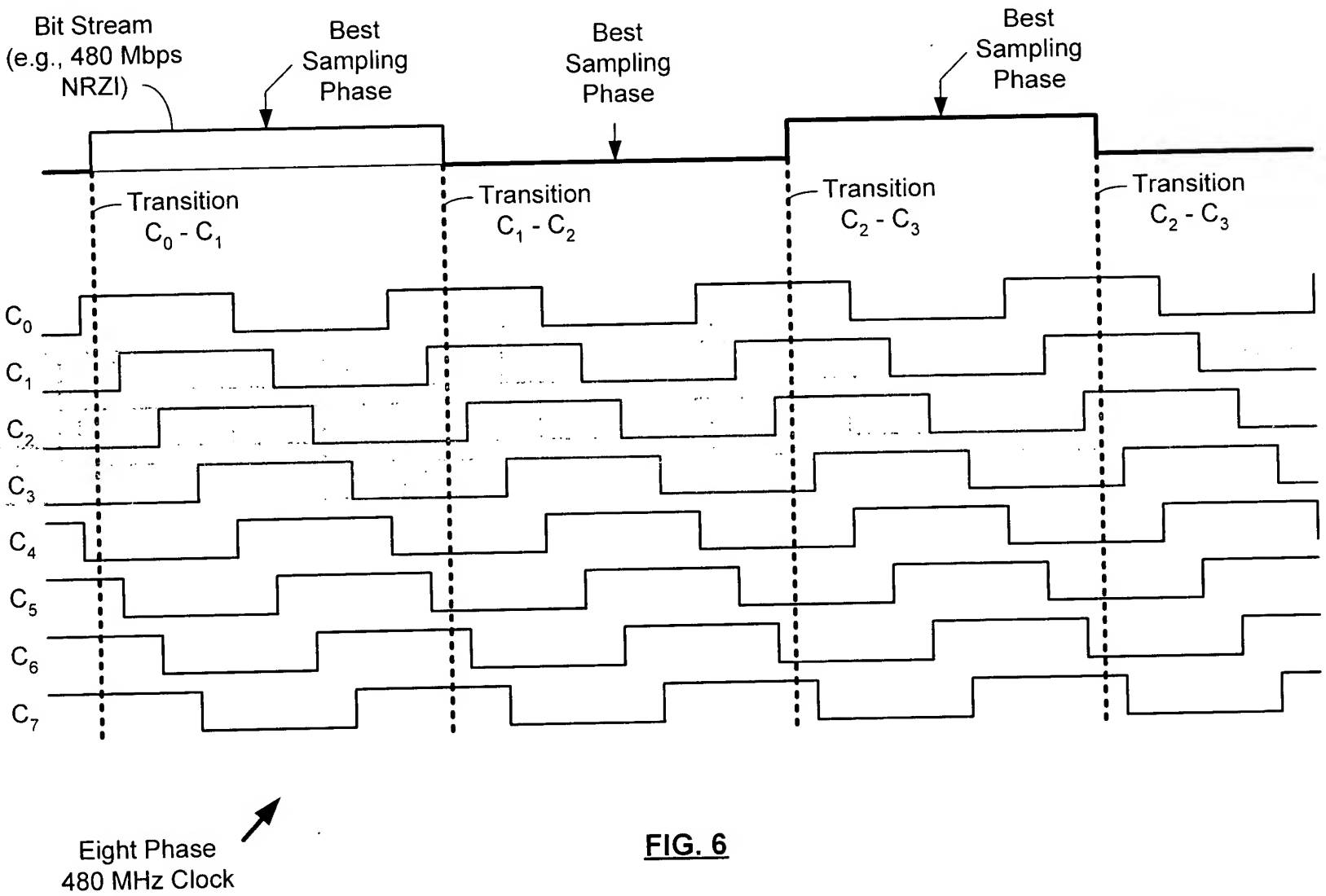
Bit Stream
(e.g., 480 Mbps
NRZI)
Best
Sampling
Phase
Best
Sampling
Phase
Best
Sampling
Phase
Transition
$C_0$ - $C_1$
Transition
$C_1$ - $C_2$
Transition
$C_2$ - $C_3$
Transition
$C_2$ - $C_3$
$C_0$
$C_1$
$C_2$
$C_3$
$C_4$
$C_5$
$C_6$
$C_7$
Eight Phase
480 MHz Clock

FIG. 6

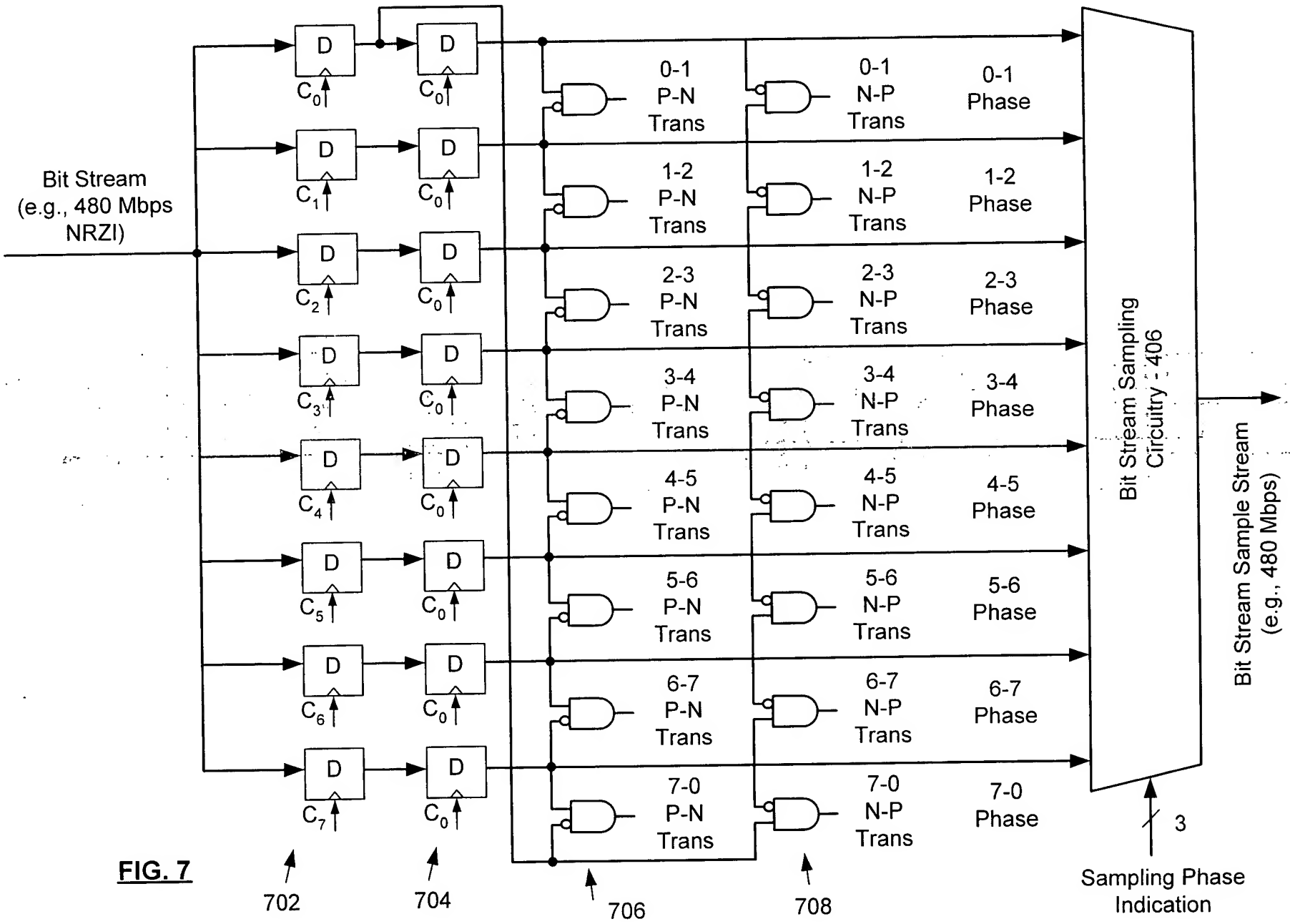
Bit Stream
(e.g., 480 Mbps
NRZI)
D
$C_0$
$C_1$
$C_2$
$C_3$
$C_4$
$C_5$
$C_6$
$C_7$
0-1
P-N
Trans
1-2
P-N
Trans
2-3
P-N
Trans
3-4
P-N
Trans
4-5
P-N
Trans
5-6
P-N
Trans
6-7
P-N
Trans
7-0
P-N
Trans
0-1
N-P
Trans
1-2
N-P
Trans
2-3
N-P
Trans
3-4
N-P
Trans
4-5
N-P
Trans
5-6
N-P
Trans
6-7
N-P
Trans
7-0
N-P
Trans
0-1
Phase
1-2
Phase
2-3
Phase
3-4
Phase
4-5
Phase
5-6
Phase
6-7
Phase
7-0
Phase
Bit Stream Sampling
Circuitry - 406
Bit Stream Sample Stream
(e.g., 480 Mbps)
3
Sampling Phase
Indication
702
704
706
708

FIG. 7

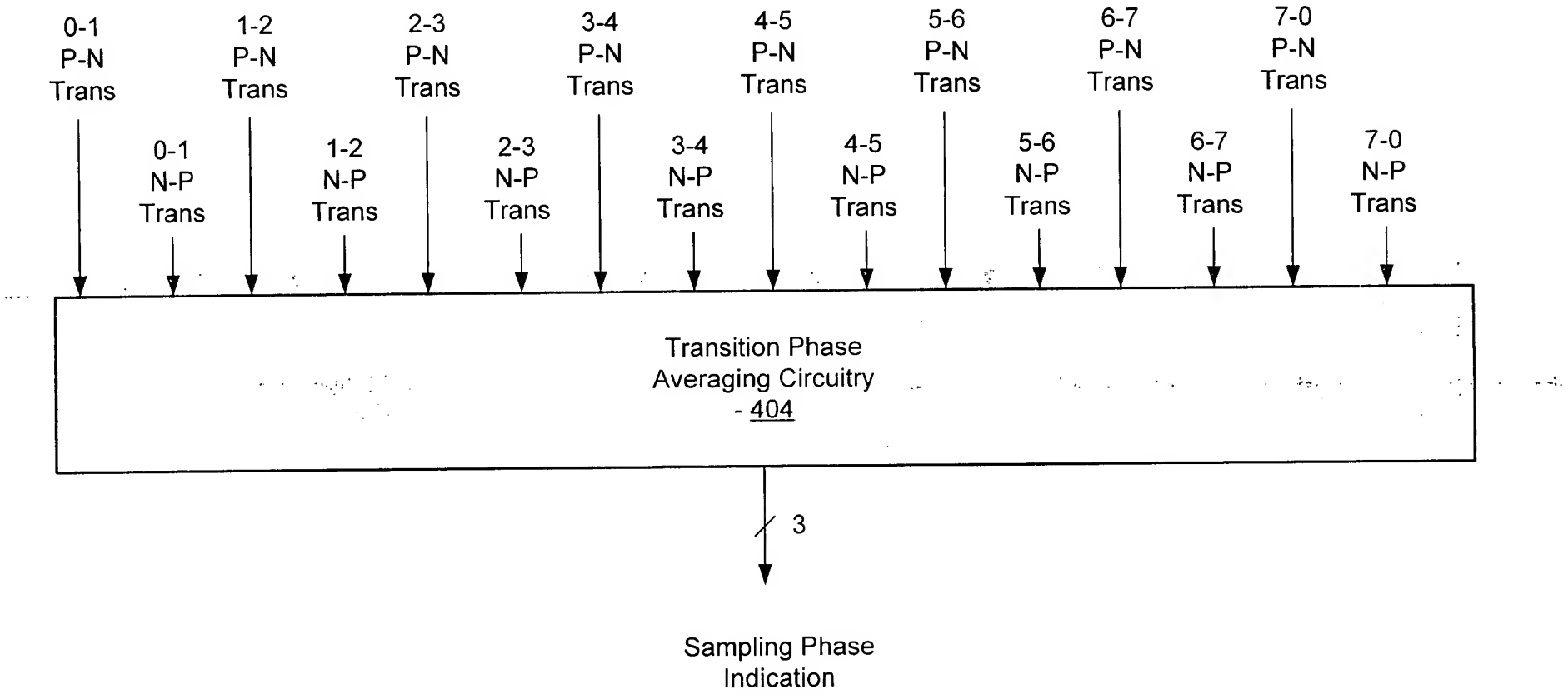
0-1 P-N Trans
0-1 N-P Trans
1-2 P-N Trans
1-2 N-P Trans
2-3 P-N Trans
2-3 N-P Trans
3-4 P-N Trans
3-4 N-P Trans
4-5 P-N Trans
4-5 N-P Trans
5-6 P-N Trans
5-6 N-P Trans
6-7 P-N Trans
6-7 N-P Trans
7-0 P-N Trans
7-0 N-P Trans
Transition Phase Averaging Circuitry - 404
3
Sampling Phase Indication

FIG. 8

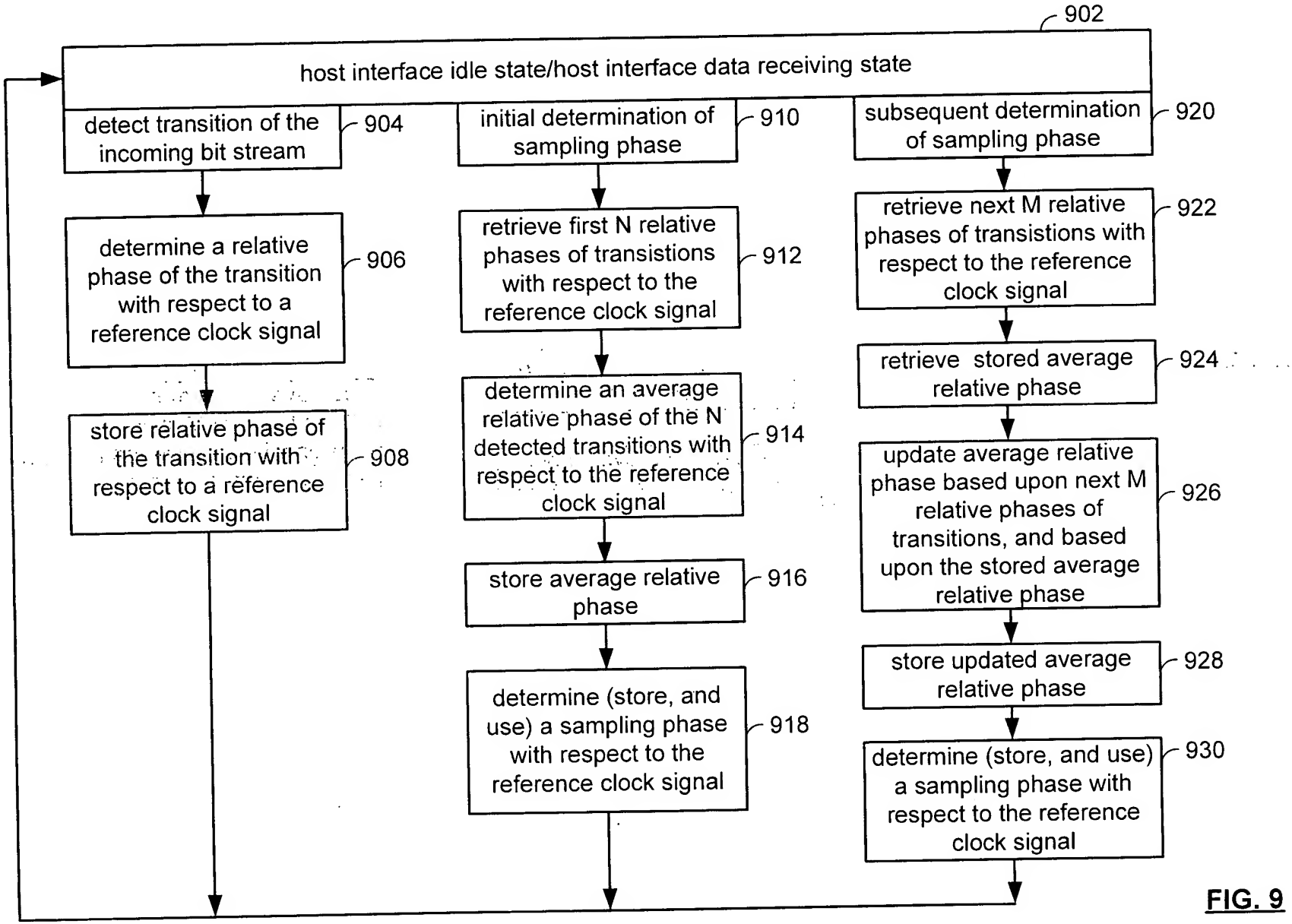
902
host interface idle state/host interface data receiving state
detect transition of the incoming bit stream
904
determine a relative phase of the transition with respect to a reference clock signal
906
store relative phase of the transition with respect to a reference clock signal
908
initial determination of sampling phase
910
retrieve first N relative phases of transistions with respect to the reference clock signal
912
determine an average relative phase of the N detected transitions with respect to the reference clock signal
914
store average relative phase
916
determine (store, and use) a sampling phase with respect to the reference clock signal
918
subsequent determination of sampling phase
920
retrieve next M relative phases of transistions with respect to the reference clock signal
922
retrieve stored average relative phase
924
update average relative phase based upon next M relative phases of transitions, and based upon the stored average relative phase
926
store updated average relative phase
928
determine (store, and use) a sampling phase with respect to the reference clock signal
930

FIG. 9

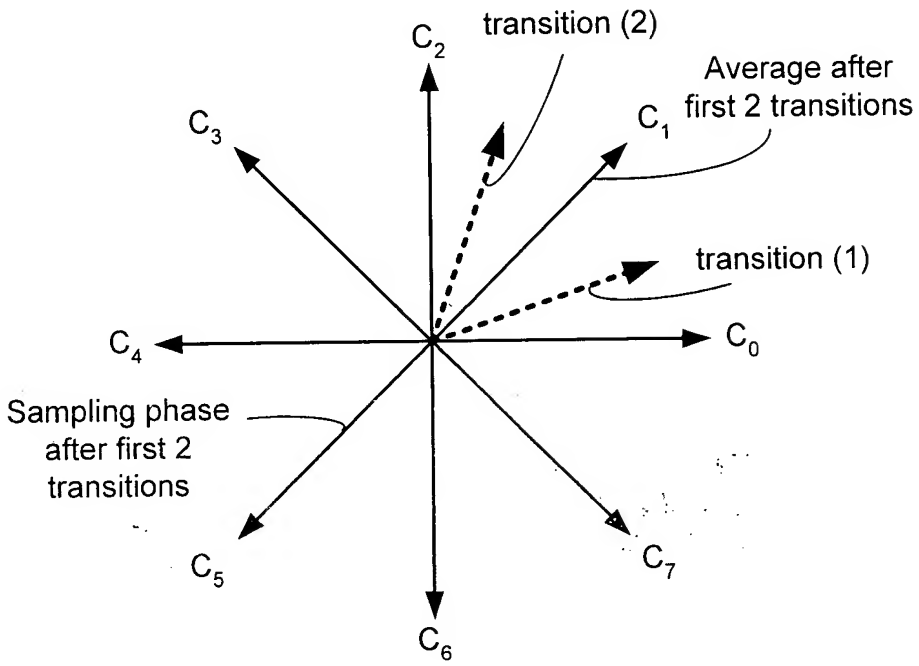


FIG. 10A

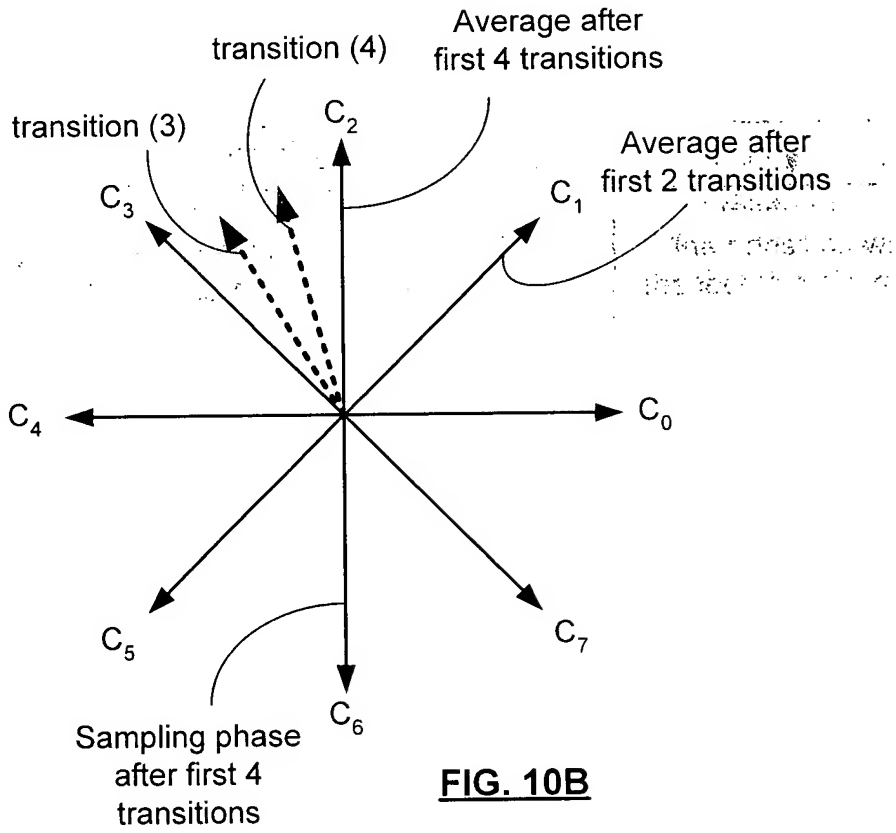


FIG. 10B

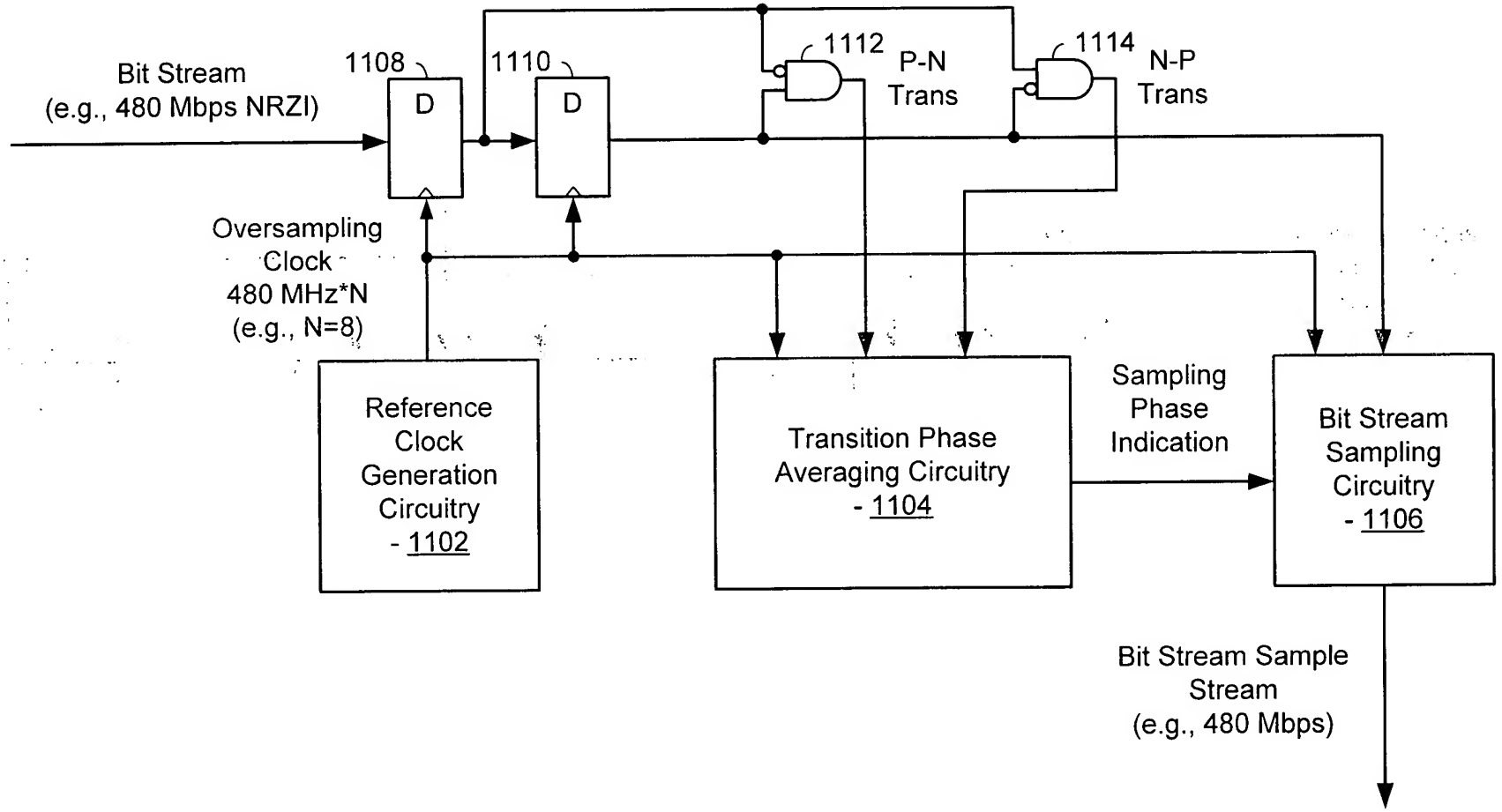
Bit Stream
(e.g., 480 Mbps NRZI)
1108
D
1110
D
1112
P-N
Trans
1114
N-P
Trans
Oversampling
Clock
480 MHz*N
(e.g., N=8)
Reference
Clock
Generation
Circuitry
- 1102
Transition Phase
Averaging Circuitry
- 1104
Sampling
Phase
Indication
Bit Stream
Sampling
Circuitry
- 1106
Bit Stream Sample
Stream
(e.g., 480 Mbps)

FIG. 11